WE CLAIM:

1. A memory cell comprising:

a substrate that comprises a first region and a second region with a channel therebetween and a gate above said channel;

a charge trapping region that contains a first amount of charge,

a layer positioned between said channel and said charge trapping region, wherein said layer has a thickness such that said first amount of charge is prevented from directly tunneling into said layer; and

a silicided bitline.

2. The memory cell of claim 1, comprising an oxide that overlies said silicided bitline.

3. The memory cell of claim 1, comprising a polysilicon layer that overlies said gate.

4. The memory cell of claim 3, comprising a silicide layer that overlies said polysilicon layer.

5. The memory cell of claim 1, wherein said charge trapping region comprises silicon nitride.

6. The memory cell of claim 1, wherein said gate comprises an N-type material.

7. The memory cell of claim 6, wherein said gate comprises a polycrystalline silicon.

8. The memory cell of claim 1, further comprising an insulating layer formed on and overlaying said charge trapping region.

9. The memory cell of claim 8, wherein said insulating layer comprises silicon dioxide.

10. The memory cell of claim 9, wherein said charge trapping region comprises silicon nitride.

11. The memory cell of claim 1, wherein said memory cell comprises an EEPROM memory cell.

12. The memory cell of claim 1, wherein said memory cell comprises a two-bit memory cell.

13. The memory cell of claim 1, wherein said substrate comprises a P-type substrate.

14. A process of fabricating a memory cell comprising a substrate that comprises a first region and a second region with a channel therebetween, the method comprising:

forming a gate above said channel of said substrate;
forming a bitline; and
siliciding said bitline.

15. The process of claim 14, comprising forming an oxide over said silicided bitline.

16. The process of claim 14, wherein prior to said forming a bitline a polysilicon layer is formed over said gate.

17. The process of claim 16, comprising siliciding said polysilicon layer.

18. The process of claim 16, wherein said siliciding of said bitline and said polysilicon layer occur simultaneously.

19. The process of claim 14, comprising:

forming a charge trapping region that contains a first amount of charge; and

forming a layer between said channel and said charge trapping region, wherein said layer has a thickness such that said first amount of charge is prevented from directly tunneling into said layer.

20. The process of claim 19, wherein said charge trapping region comprises silicon nitride.

21. The process of claim 14, wherein said gate comprises an N-type material.

22. The process of claim 21, wherein said gate comprises a polycrystalline silicon.

23. The process of claim 19, further comprising forming an insulating layer on said charge trapping region.

24. The process of claim 23, wherein said insulating layer comprises silicon dioxide.

25. The process of claim 24, wherein said charge trapping region comprises silicon nitride.

26. The process of claim 14, wherein said memory cell comprises an EEPROM memory cell.

27. The process of claim 14, wherein said memory cell comprises a two-bit memory cell.

28. The process of claim 14, wherein said substrate comprises a P-type substrate.

29. The process of claim 14, further comprising scaling the length of said bitline.

30. The process of claim 29, wherein said scaling comprises reducing the thermal cycle of said bitline.